NPSAT1 80196 Microcontroller Kernel

Introduction

NPSAT1 is a low-cost, technology demonstration satellite hosting a number of experiments. Commercial, off-the-shelf (COTS)-based technology will be implemented with custom designs to offer a low-cost command and data handling (C&DH) subsystem building on commercial, desktop PC architecture and standards-based specifications. In addition to an experimental C&DH subsystem, NPSAT1 will demonstrate the use of non-volatile ferroelectric RAM which is inherently radiation-tolerant and lithium-ion polymer batteries, state-of-the-art technology that will be employed offering high energy density (Watt-hr/kg) for space applications.

Experiments on-board NPSAT1 include two Naval Research Laboratory (NRL) payloads. The coherent electromagnetic radio tomography (CERTO) experiment and a Langmuir probe. The CERTO experiment is a radio beacon which, in concert with ground station receivers, is used to measure total-electron-content (TEC) in the ionosphere. The Langmuir probe will augment CERTO data by providing on-orbit measurements. The other experiments are of NPS origin. These include a novel design for a spacecraft computer board, a COTS visual imager (VISIM), and some micro-electromechanical systems (MEMS)-based rate sensors.

NPSAT1 Microcontroller Subsystems Description

NPSAT1 contains three microcontroller-based subsystems. One is responsible for maintaining the Electrical Power Subsystem (EPS), another operates the Attitude Control Subsystem (ACS), and the third controls the Solar Cell Measurement Subsystem (SMS). An UTMC 80C196KD version of the 80196 microcontroller is used. Each subsystem has unique hardware with which to interface. And, each of these subsystems is connected to the Command and Data Handler (C&DH) central computer system via an asynchronous serial link.

Description of Thesis Topics

Although each of these microcontroller-based subsystems performs vastly different tasks they all have a need for a common kernel. The 80196 kernel will consist of common hardware initialization code, A/D and timer handlers, a communication protocol, and a command interface which operates on top of the communication link.

This thesis will develop the design, implementation, testing, and documenting of the common 80196 kernel. The software will be developed in C and also possibly C++ as well possibly a small amount of 80196 assembly language. Tools available are the IAR for 80196 embedded system development software which runs under Windows.

Proposed Outline

- NPSAT1 Introduction
- Subsystem logic requirements
- Kernel requirements

- Software design and implementation
- Conclusions & Recommendations
- Appendix of Test Results, Test Data, Software

Suggested References

- NPSAT1 PDR Slides
- Intel 80C196KC/80C196KD User's Manual.
- "Overview of the NPSAT1 Spacecraft Architecture and Technology Demonstration Satellite," D. Sakoda and J. Horning, Paper SSC02-I-4, 16th Annual AIAA/USU Conference on Small Satellites, Logan, UT 2002.